In the Claims:

1-11 (Canceled).

12 (Currently amended): A circuit arrangement for a communication system for terminating a plurality of interfaces at a common bus and for generating a synchronization clock for synchronizing the bus, comprising:

a first multiplexer ~~which can be~~ controlled by a first control signal with a plurality of inputs corresponding to a plurality of transmission lines of the interfaces;

a respective phase control unit, preceding each input of the first multiplexer, which derives a respective clock generator signal from ~~the~~ a received signal of the corresponding transmission line;

where the clock generator signal of one of the transmission lines ~~can be~~ is switched through as output signal of the first multiplexer in dependence on the first control signal;

a phase locked loop, at the inputs of which the output signal of the first multiplexer and a clock from a clock generator ~~which can be~~ operated with an external ~~oscillating~~ crystal oscillator, are present and at the output of which an internal reference clock is present which is generated from the clock generator signal and the clock from the clock generator;

an output connection from the clock from the clock generator;

a second multiplexer, ~~which can be~~ controlled by a second control signal, at the inputs of which the output signal of the phase locked loop and a reference clock, ~~which can be~~ supplied externally, are present;

where one of the input signals of the second multiplexer ~~can be~~ is switched through as output signal of the second multiplexer in dependence on the second control signal; and

a clock divider unit, following the second multiplexer for generating the synchronizing clock from the output signal of the second multiplexer.

13 (Currently amended): The circuit arrangement as claimed in claim 12, characterized in that the clock generator signal ~~can be~~ is generated by a combination of the received signals of at least two transmission lines of the interfaces, particularly by averaging.

14 (Currently amended): The circuit arrangement as claimed in claim 12, characterized in that signals which ~~can be~~ are transmitted via the transmission lines of the interfaces correspond to an ~~the U~~ interface protocol of ISDN.

15 (Currently amended): The circuit arrangement as claimed in claim 13, characterized in that signals which ~~can be~~ are transmitted via the transmission lines of the interfaces correspond to the ~~U~~ interface protocol of ISDN.

16 (Currently amended): The circuit arrangement as claimed in claim 12, characterized in that signals which ~~can be~~ are transmitted via the transmission lines of the interfaces correspond to an XDSL protocol.

17 (Currently amended): The circuit arrangement as claimed in claim 13, characterized in that signals which ~~can be~~ are transmitted via the transmission lines of the interfaces correspond to an XDSL protocol.

18 (Previously presented): The circuit arrangement as claimed in claim 16, characterized in that the XDSL protocol corresponds to an ADSL or SDSL or VDSL or HDSL protocol.